Behavioral Modeling of RF and Microwave Circuit Blocs for Hierarchical Simulation of Modern Transceivers.

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***Abstract* — The development of simulation and macro-modeling techniques for RF and microwave communication systems has been a high priority research subject for several years. If one observed this last years an impressive improvement of simulation tools performances, the full chip simulation of modern TX-RX chains remains a real stumbling block, as the transistor count has considerably increased. This paper discusses the hierarchical RF simulation issue using the same Harmonic Balance or Envelope Transient simulation engine for both transistor level description and circuit bloc macro-models. This method can reduce the size of the problem to enable accurate and fast simulation of large size circuits. The concept requires however to develop macro-modeling techniques taking into account impedance mismatch effects, which are discussed here.**

***Index Terms* — Behavioral modeling, Envelope Transient, Harmonic Balance, hierarchical simulation, impedance mismatch, Volterra series.**

I. Introduction

In the two last decades, many advances have been realized on the modeling and simulation techniques for RF and microwave circuits. This work has led to tremendously powerful design and verification tools for communication system design. However in the meantime the circuit complexity has considerably increased in the new generations of RF transceivers (TX-RX) that show transistor count in the several thousands, whether in a single or multiple chips [1]. The classical flattened transistor level simulation of the transceiver, especially on parasitic extraction views, thus requires tremendous memory resources and overly long computation time, making circuit design and verification extremely painful.

The first solution that comes in mind for circumventing this problem is to use techniques that reduce the complexity order of the system or part of the system while keeping the best compromise between computational efficiency and accuracy. This complexity order reduction is often termed as behavioral modeling or macro-modeling. The basic idea is to allow the designer to combine transistor level descriptions (for critical sections) with circuit-bloc macro-models (for the idle sections) within the common Harmonic Balance (HB) and Envelope Transient (ET) engines. This leads to the concept which we term herein "hierarchical simulation" to imply that each macro-model is eligible to be built directly while running the HB/ET engine, by triggering a lower hierarchy HB/ET engine. In this paper however, we will consider the simpler case where the circuit-bloc macro-model is built offline. An important point with the macro-model to be used here is that it has to account the impedance mismatch effects at the circuit bloc ports. There has recently been an important amount work on nonlinear circuit-bloc macro-modeling [2]-[10]. This work however targets classical data flow system level simulation and thus focuses mainly on nonlinearity and memory effects. A few works have discussed the impedance mismatch issues [11]-[13], but then ignored pass band memory effects. Finally, we have some works based on more direct model order reduction (MOR) and neural networks approach, that are potentially more effective, but the net gain in complexity reduction is insufficient [14].

In this paper we will consider the black box concept of "nonlinear S parameter (hot S)" proposed by J. Verspecht [12]. We will provide the mathematical foundation of the concept through the formalism of dynamic Volterra series expansion to extend its usage to systems with band-pass memory. We will then present a simulation example of a receive chain, combining transistor level and circuit-bloc level descriptions, that indicates the accuracy of the proposed model and efficiency of the hierarchical simulation approach.

II. Extension of Linear Scattering Functions to Nonlinear Case using the Volterra Theory

The general laws governing a two-port subsystem is expressed in (1), where $\hat{b}_i(t)$ and $\hat{a}_i(t)$ are the complex envelope of respectively the reflected and incident power waves on the port number $i=1,2$, and the star exponent indicates the complex conjugate of the variable .

$$\begin{aligned}\hat{b}_1(t) &= \mathbb{F}_{NL1}\left(\hat{a}_1(t),\hat{a}_1^*(t),\hat{a}_2(t),\hat{a}_2^*(t),t\right)\\ \hat{b}_2(t) &= \mathbb{F}_{NL2}\left(\hat{a}_1(t),\hat{a}_1^*(t),\hat{a}_2(t),\hat{a}_2^*(t),t\right)\end{aligned} \tag{1}$$

It has to be understood that we are making the assumption that the signal at each port i is a band-pass signal centered around a carrier frequency ω_i such that

$$\begin{aligned}a_i(t) &= \Re e[\hat{a}_i(t)e^{j\omega_i t}]\\ b_i(t) &= \Re e[\hat{b}_i(t)e^{j\omega_i t}]\end{aligned} \tag{2}$$

This assumption holds well for many circuit blocs like amplifiers, mixers and filters. Equation (1) can be straightforwardly extended to a larger number of ports. Without loss of generality, considering a sufficiently small sampling time step, the outputs of the two-port subsystem with memory at time instant t_n can be expressed in a discrete form as follows:

$$\begin{aligned}\hat{b}_1(t_n) &= \mathbb{F}_{NL1}\left(\hat{a}_1(t_n),\cdots,\hat{a}_1^*(t_{n-M}),\hat{a}_2(t_n),\cdots,\hat{a}_2^*(t_{n-M})\right)\\ \hat{b}_2(t_n) &= \mathbb{F}_{NL2}\left(\hat{a}_1(t_n),\cdots,\hat{a}_1^*(t_{n-M}),\hat{a}_2(t_n),\cdots,\hat{a}_2^*(t_{n-M})\right)\end{aligned} \quad (3)$$

In the linear case, these equations simply reduce to the scattering function notion or S parameters [15]. In the nonlinear case however, the superposition theorem is unworkable and the idea here is to apply a dynamic Volterra series expansion to (3), as it has been recently considered in references [3]-[5] for system level model type (i.e., impedance matched conditions: $b_1(t)=a_2(t)=0$). Since in practice, the amplifier or mixer bloc should work close to the impedance matching conditions, we will assume that the incident waveform $a_2(t)$ at the output, will be relatively small, so that the relation defined by equation (3) behaves linearly as to $\hat{a}_2(t)$ and $\hat{a}_2^*(t)$. This assumption is to say that the bloc nonlinearity is only governed by the incident wave at the input port. With this assumption, we may now judiciously carry a power series expansion of (3) around a trajectory defined by $a_1(t_{n-k})=a_1(t_n)\ \forall k$ and $a_2(t_{n-k})=0\ \forall k$. Considering the assumption of weak $a_2(t)$ and the assumption of short memory duration of the circuit bloc as compared to the signal envelope speed (that is usually valid in narrow modulation bandwidth applications), we may limit the power expansion to first order, and straightforwardly derive the following expression of reflected waveforms.

$$\begin{aligned}\hat{b}_i(t) &= S_i^0\left(\left|\hat{a}_1(t)\right|\right)\hat{a}_1(t)\\ &+\frac{1}{2\pi}\int_{-\infty}^{+\infty} S_{i1}^{\oplus}\left(\left|\hat{a}_1(t)\right|,\Omega\right).\hat{A}_1(\Omega).e^{j.\Omega.t}.d\Omega\\ &+\frac{1}{2\pi}\int_{-\infty}^{+\infty} S_{i2}^{\oplus}\left(\left|\hat{a}_1(t)\right|,\Omega\right).\hat{A}_2(\Omega).e^{j.\Omega.t}.d\Omega\\ &+\frac{1}{2\pi}\int_{-\infty}^{+\infty} S_{i1}^{\Delta}\left(\left|\hat{a}_1(t)\right|,-\Omega\right).\hat{A}_1^*(\Omega).e^{j.2.\varphi_{\hat{a}1}(t)}.e^{-j.\Omega.t}.d\Omega\\ &+\frac{1}{2\pi}\int_{-\infty}^{+\infty} S_{i2}^{\Delta}\left(\left|\hat{a}_1(t)\right|,-\Omega\right).\hat{A}_2^*(\Omega)e^{j.2.\varphi_{\hat{a}1}(t)}.e^{-j.\Omega.t}.d\Omega\end{aligned} \quad (4)$$

In this expression $\left|\hat{a}_1(t)\right|$, $\varphi_{\hat{a}1}(t)$ and $\hat{A}_1(\Omega)$ stand respectively for the magnitude and the phase of the incident wave envelope $\hat{a}_1(t)$ and its frequency spectrum.

We may observe that (4) is an extension of the model expression reported in [4], that handles both input and output impedance mismatch, through the dependence to both input and output incident waves. The circuit bloc is thus characterized by the static Volterra kernels $S_i^0\left(\left|\hat{a}_1(t)\right|\right)$ and the dynamic kernels $S_{ij}^{\oplus}\left(\left|\hat{a}_1(t)\right|,\Omega\right)$ and $S_{ij}^{\Delta}\left(\left|\hat{a}_1(t)\right|,\Omega\right)$ which are a function of the input incident wave only. These smoothly extend the notion of scattering functions to nonlinear behavior.

In fact if we write $\hat{a}_1(t)=\frac{1}{2\pi}\int_{-\infty}^{+\infty}\hat{A}_1(\Omega)e^{j\Omega t}d\Omega$ and express the reflected waves $\hat{b}_i(t)$ using a time varying spectrum as a result of the nonlinear dynamics of the circuit bloc : $\hat{b}_i(t)=\frac{1}{2\pi}\int_{-\infty}^{+\infty}\hat{B}_i(t,\Omega)e^{j\Omega t}d\Omega$, we can rewrite (4) in the more familiar scattering functions form below.

$$\begin{bmatrix}\hat{B}_1(t,\Omega)\\ \hat{B}_2(t,\Omega)\end{bmatrix}=\left[S^{\oplus}\right].\begin{bmatrix}\hat{A}_1(\Omega)\\ \hat{A}_2(\Omega)\end{bmatrix}+\left[S^{\Delta}\right].\begin{bmatrix}\hat{A}_1^*(-\Omega)\\ \hat{A}_2^*(-\Omega)\end{bmatrix} \quad (5)$$

with $\left[S^{\oplus}\right]=\begin{bmatrix}S_1^0\left(\left|\hat{a}_1(t)\right|\right)+S_{11}^{\oplus}\left(\left|\hat{a}_1(t)\right|,\Omega\right) & S_{12}^{\oplus}\left(\left|\hat{a}_1(t)\right|,\Omega\right)\\ S_2^0\left(\left|\hat{a}_1(t)\right|\right)+S_{21}^{\oplus}\left(\left|\hat{a}_1(t)\right|,\Omega\right) & S_{22}^{\oplus}\left(\left|\hat{a}_1(t)\right|,\Omega\right)\end{bmatrix}$

and $\left[S^{\Delta}\right]=e^{j.2.\varphi_{\hat{a}1}(t)}.\begin{bmatrix}S_{11}^{\Delta}\left(\left|\hat{a}_1(t)\right|,\Omega\right) & S_{12}^{\Delta}\left(\left|\hat{a}_1(t)\right|,\Omega\right)\\ S_{21}^{\Delta}\left(\left|\hat{a}_1(t)\right|,\Omega\right) & S_{22}^{\Delta}\left(\left|\hat{a}_1(t)\right|,\Omega\right)\end{bmatrix}$

Equation (5) defines the notion of **nonlinear S parameters**. In small signal conditions, the term $\left[S^{\Delta}\right]$ vanishes and the remaining term $\left[S^{\oplus}\right]$ reduces to the conventional S parameters independent on the input amplitude and thus on the time. Note that when the circuit is memoryless within the signal bandwidth, the S parameters are independent on the frequency and (5) reduces to the "hot" S parameters concept postulated in [12].

Here it is worth noting that the term "nonlinear S parameters" is commonly used in many simulation tools to designate the equation (5) where the term $\left[S^{\Delta}\right]$ is ignored. This may lead to significant errors when used to determine optimum load matching and stability conditions.

III. Extraction of the Nonlinear S Parameters

From equation (4) and reporting to reference [4], it is easily shown that the S parameters terms in (5) are unambiguously determined by the setup sketched in reference [4], where the circuit bloc is driven by a two-tone signal $a_1(t)=\Re e\left[(A_1+\delta A_1.e^{j\Omega t}).e^{j\omega_1 t}\right]$, $\left|\delta A_1\right|<<1$ and loaded with three different impedances as described in [12]. To fully characterize the circuit bloc, the amplitude A_1 of the incident

wave is swept from small signal operation to saturation, and the frequency of the small tone Ω is swept thought the bloc operation bandwidth.

IV. Application – Hierarchical Simulation

The model equation as defined by (4) can hardly be implemented in time domain circuit simulators as it is a band pass formalism. In the other hand, this fits well with Harmonic Balance and Envelope Transient simulators, as they directly handle frequency domain information. The corresponding Volterra integral can be efficiently computed by polynomial and Padé decompositions.

As an application example, we have integrated this new model in the Xpedion's GoldenGate™ simulator and applied it to the simulation of a BiCMOS RX chain, Figure 1. In this simulation we have modeled the LNA and the mixer with the above described model and carried the simulation of the chain in the 3 scenarios (a), (b) and (c) depicted in Figure 1 below (transistor level bench, mix transistor/circuit-bloc level bench and circuit-bloc level bench). We have then compared the simulation results for the 3 benches.

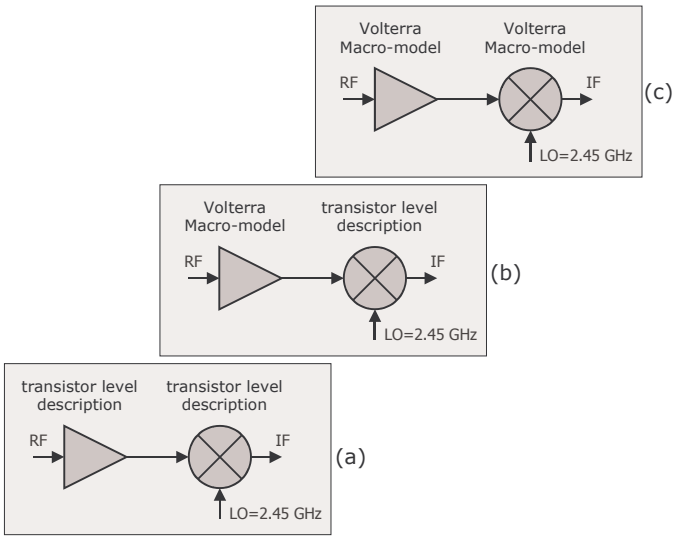

Figure 1 : example of hierarchical simulation : (a) transistor level bench, (b) mix transistor/circuit-bloc level bench, (c) circuit-bloc level bench

Figure 2 shows the power gain curve of the RX when it is driven by a sinusoidal signal (frequency = 2.45 GHz). Figure 3 shows the IM3 curve of the RX for a tone spacing equal to 1 MHz. Finally, Figure 4 shows the ACPR plot of the RX in zero IF conditions when it is driven by a WCDMA signal @ 3.84 MB/s. We have also plotted in these figures, the result obtained when the impedance mismatch effects are ignored in the amplifier macro-model.

All these plots show that the model proposed is accurate and that neglecting impedance mismatch can lead to important errors in both gain compression and ACPR prediction (up to 2dB).

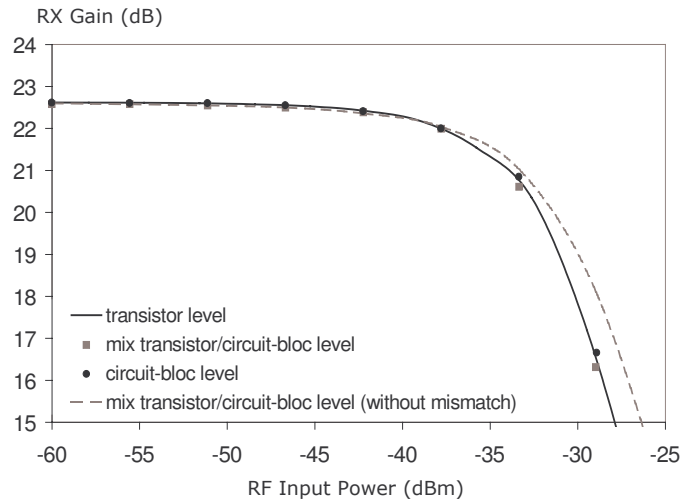

Figure 2 : RX Gain compression

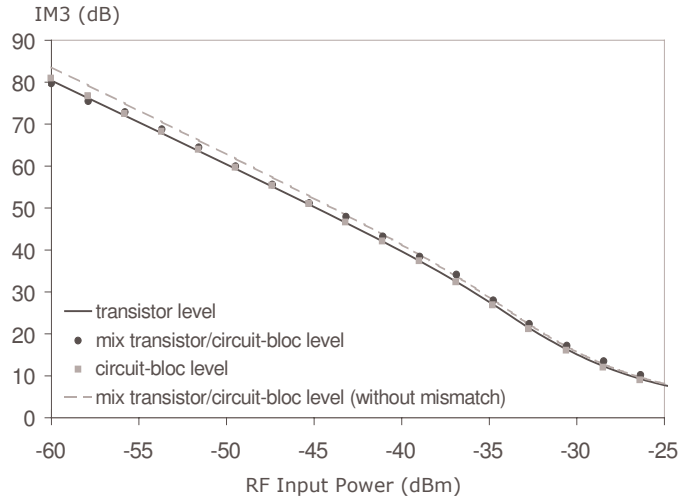

Figure 3 : IM3 of RX, tone-spacing @ 1 MHz

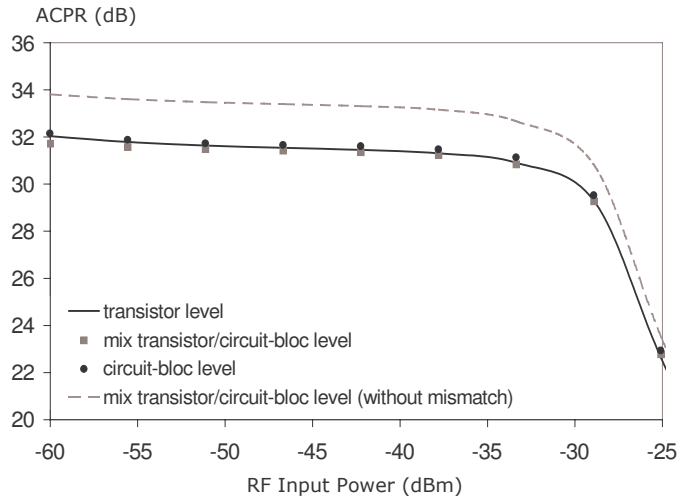

Figure 4 : ACPR of RX , WCDMA signal @ 3.84 MB/s

The simulation performances (memory and CPU) are summarized in the table I below. We observe that using the macro-model has reduced the memory usage and CPU time by a factor which is roughly the circuit node reduction ratio. For example in bench (b), the original circuit had about N1=2400 nodes which has been reduced to about N2=1400 nodes in the mixed mode (i.e. basically the number of nodes in the mixer), hence the reduction in CPU and memory concords with the node reduction factor N2/N1≅0.6. Finally the performances in circuit-bloc level bench (c) show a simulation speed up of many orders, without sacrificing accuracy. Hierarchical simulation thus provides to the circuit designer a great simulation flexibility.

TABLE I
SIMULATIONS PERFORMANCES

	memory usage			simulation time		
	transistor level	mix level	circuit-bloc level	transistor level	mix level	circuit-bloc level
power gain	220 MB	150 MB	15 MB	6 min.	4 min.	4 sec.
IM3	550 MB	350 MB	18 MB	1 h.	39 min.	30 sec.
ACPR	200 MB	140 MB	15 MB	2 h. 30min.	1 h. 30 min.	24 sec.

VI. CONCLUSION

This paper has presented a new macro-modeling principle for nonlinear RF and microwave circuit blocs that has shown to be fairly simple to generate and accurate. This accounts well of the nonlinearity and impedance mismatch effects which are important for intermodulation distortion prediction. The model is based on a theoretically sound approach through the Volterra series expansion of the general laws governing a two-port bloc and has led to a rigorous derivation of the concept of nonlinear S parameters which is important in PA and mixer design. This model enables to reduce the number of nodes of a circuit bloc to only a few units, irrespective of the original number. The tests carried on a Bi-CMOS RX has shown that using this model conserves convergence properties of HB engine into deep saturation. It is therefore an important contribution for the simulation of modern TX-RX chains.

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