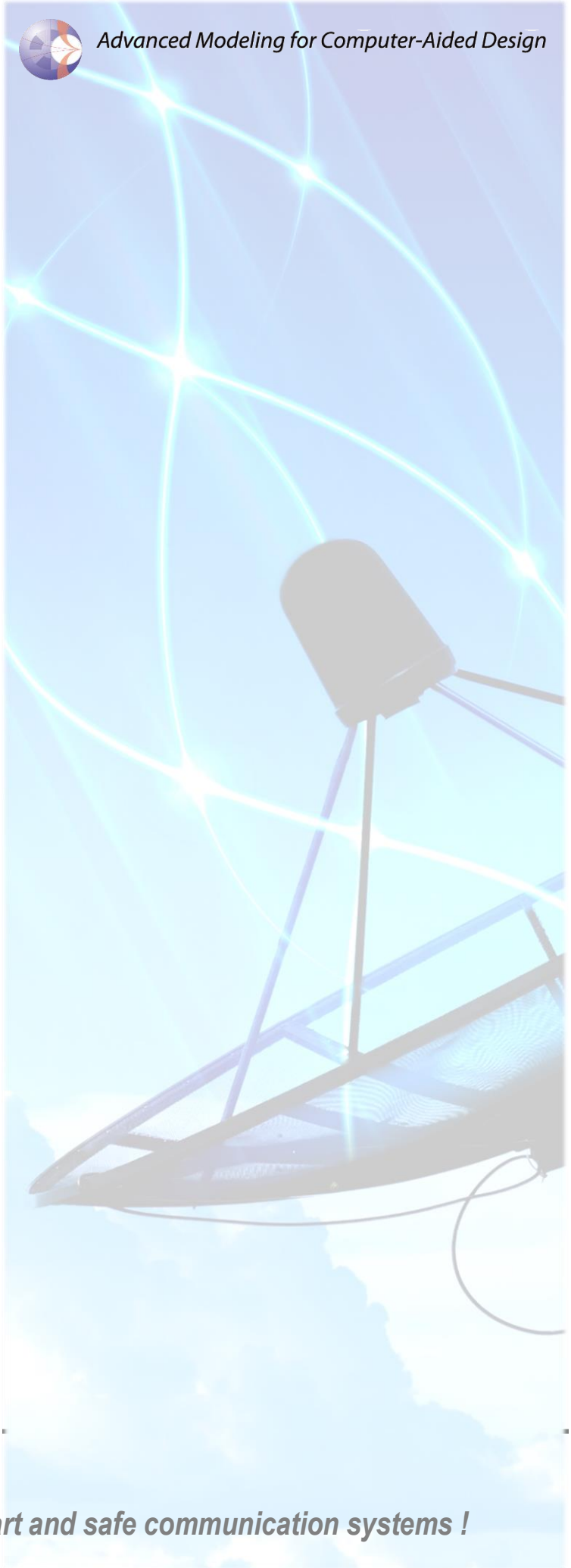
AMCAD Engineering

White Paper

Advanced Modeling for Computer-Aided Design

Behavioral modelling challenges for RF system simulation



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Behavioral modelling challenges for RF system simulation

Introduction

The fast and ever-increasing demand for high-speed data services has been motivating and leading to define the next generation of cellular mobile communications, referred to as 5G New Radio. To take advantage of the opportunities offered by 5G NR, methods and techniques to design telecommunication systems must continue to evolve to meet, on the one hand, the spectral and energy efficiency requirements and, on the other hand, cost and time to market reduction.

Current research proposes significant developments to achieve higher transmission rates—first, the use of Millimeter-wave bands, which gives access to larger frequency bandwidths. Second, deployment of new transmission techniques, to be integrated into future 5G radio interfaces, including multi-level modulation schemes and multi-carrier (MC) technologies such as Filter Bank Multicarrier (FBMC) or variants of Orthogonal Frequency-division Multiplexing (OFDM). One of the fundamental problems in the application of these techniques is the strong amplitude fluctuation present in the time domain representation of the signal, resulting in a high Peak to Average Power Ratio (PAPR). The high value of PAPR linked to the presence of non-linear elements in the transmission chain, particularly Power Amplifiers (PA), leads to in-band and out-of-band signal distortions, as well as a degradation of the Bit Error Rate (BER).

Problematic

The Power amplifier represents one of the most critical elements in telecommunication systems. As the primary energy consumption circuit, it has the most significant impact on the overall efficiency of wireless transmitters. In other words, an efficient PA reduces the power consumption cost of a base station and increases the battery life of a mobile transmitter. For such, the PA should work in its saturation region. However, increasing the efficiency degrades the linearity and creates signal distortion at the output.

Indeed, the linearity of a highly compressed and efficient power amplifier is sufficiently low to require some sort of error correction. Nowadays, the methods of linearization are mature, particularly digital pre-distortion techniques (DPD), which are the most popular. System Designers or PA manufacturers can choose from a variety of commercial solutions to improve the performance of their amplifier modules or implement their custom DPD solution. However, although offering good performance, the DPD has a high cost. The implementation of a DPD system requires substantial engineering resources and system knowledge to assemble the different digital and analog parts. Indeed, this requires the use, on the one hand, of high-performance DSP units, and on the other hand, analog RF components such as mixers or ADC / DAC (Fig.1). Added to this are the various challenges that emerging applications bring. First, the new 5G standards and markets call for increasingly broadband linearization that traditional DPDs are

unable to provide. Secondly, the active antenna architectures no longer make it possible to accommodate DPD systems both in terms of form factor and overall consumption.

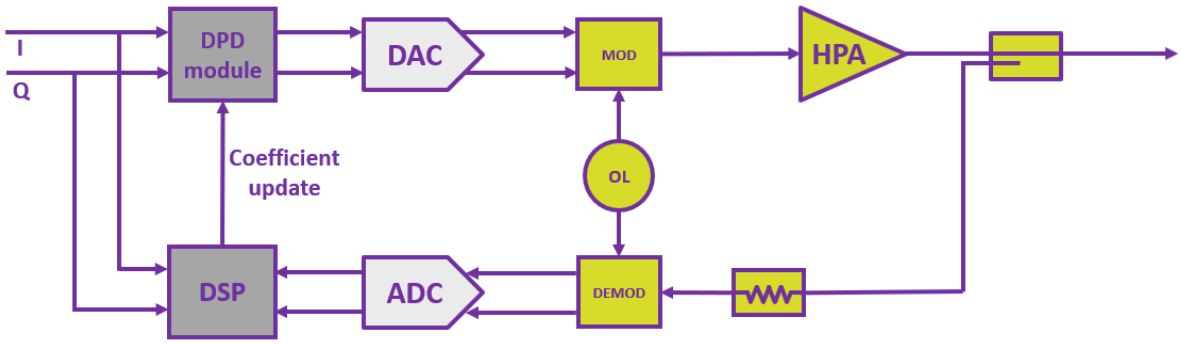

Figure 1- DPD system topology

DPD is, therefore, proving to be a critical technological challenge in new generations of communication systems and is the subject of significant financial and human R&D investment. In practice, DPD development follows specific steps which can be summarized hereunder:

- Step 1: Evaluation of the DPD algorithm in simulation

- Step 2: Implementation of the algorithm on an ASIC or an FPGA

- Step 3: Verification of the DPD system in a real situation using a PA module

Each step is essential to the final development and involves several specialized engineers, especially in design, simulation, and measurement, which leads to a high development cost. Test benches are implemented for each step to speed up development. However, if the DPD system does not meet the linearization requirements of the PA, a new iteration is necessary. It can considerably increase costs and time to market, which can jeopardize the viability of the project. The observed mismatch between simulation and measurement results can be explained by the use of simple behavioral models of PA during “step 1” of the design flow.

To assess the impact of Power Amplifiers on the baseband modulation, engineers use data-flow simulation environments. These simulators offer advanced 5G signal libraries, time, and spectrum-based analysis (BER, SER, ACPR) as well as analytical RF circuit models. However, these models prove to be insufficient to represent the nonlinearity, the frequency dispersion, and the memory effects of PA at the same time.

To deal with such challenges, many research groups focused on behavioral modeling to simulate complex designs and predict their performances under modulated signals in data flow simulators.

Illustration

Highlighting nonlinearity and memory effects

To illustrate the need for behavioral modeling, we use an amplifier design available in ADS / Keysight Technologies. This design is based on an RF transistor for mobile phone applications that can deliver 30 dBm output power in the 800 MHz band.

To highlight the impact of nonlinearity and memory effects on the model, we apply a 2-tone test signal to the circuit design (Fig. 2).

This type of signal is very well suited to analyze the distortions caused by memory effects. Indeed, a 2-tone signal, at frequencies f1 and f2, allows creating a basic envelope modulation with a PAPR of 3dB. InterModulation Distortion (IMD) is measured to indicate the circuit's nonlinearity for different input power levels and tones spacing. The envelope modulation speed is proportional to the spacing f2-f1. By probing the behavior of the circuit over a whole power range, and for different envelope modulation speeds, we are thus able to understand the behavior of the circuit under test and highlight different memory effects that characterize it. The resulting behavioral model of the circuit is then a serious candidate to simulate the realistic and reliable response of the circuit under test when stimulated with multi-carrier signals, with larger PAPRs, or wideband 5G signals.

Non-linear RF amplifiers can broadcast signals in adjacent channels and/or frequencies, causing interferences based on the same phenomena as the third-order intermodulation for two-tone input signals. Fortunately, the distortion is relatively easy to spot for such a basic stimulus.

Input power is swept up to a 4 dB gain compression point, and the frequency offset between the two tones is swept from 20 kHz to 30 MHz to probe the circuit memory effects. Beyond 30 MHz tones spacing, low-frequency memory effects have no impact on the circuit response in this example.

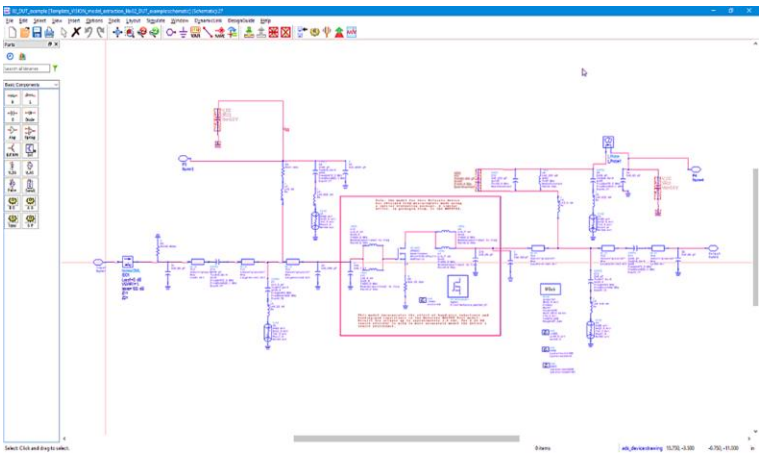

Figure 2- Original Circuit design used to extract the reference data of the behavioral power amplifier model

Using Harmonic Balance (HB), we compute the third-order intermodulation (IMD3) at the output of the circuit. An amplifier in which we would have no memory effect would give a perfectly balanced power

level response of the left and right IMDs (no hysteresis phenomenon observable on the Pout / Pin curve as a function of the modulation speed).

In our case, we observe an asymmetry between the left and right IMD3 and, more particularly, resonance on the IMD3-right, indicating the memory effects (Fig. 3).

This circuit simulation uses a non-linear electrothermal transistor model, which by its nature, includes the real memory phenomena observed in the circuit. However, the simulation convergence cannot always be achieved when cascading multiple circuits for system architecture design purposes. Therefore, creating a behavioral model of the amplifier (transistor associated with the matching and bias circuits) enables performant simulations, in terms of speed and convergence. Systems with potentially a large number of circuits can benefit from this technique because one does not need to run a "circuit-system" co-simulation, which does increase the complexity drastically.

In the extraction process of the behavioral model of the PA, simulation results serve as a reference for the validation.

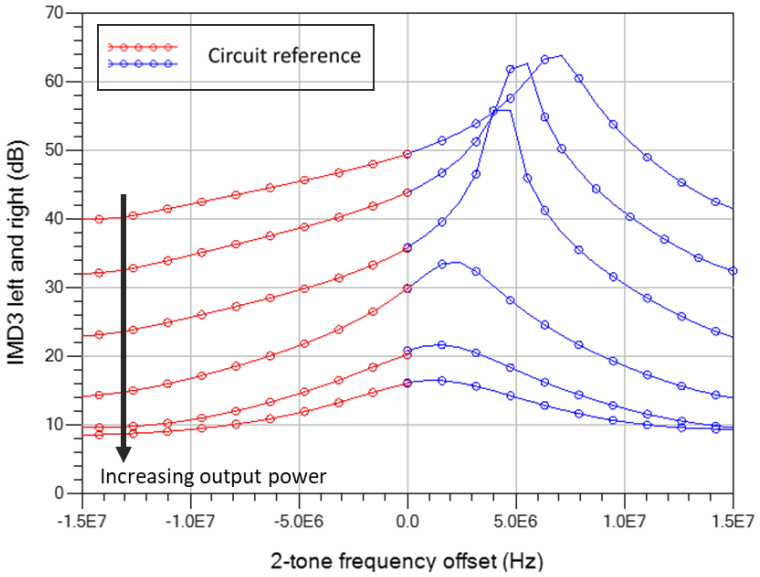

Figure 3 - 2-tone test from HB simulation. IMD3 Left in blue and IMD3 Right in red versus 2-tone spacing

Limitation of PHD model

The PHD model is a black box modeling technique initially developed for microwave components and systems [2]. The extraction of such a model uses HB simulation results, and consists of non-linear spectral mapping of the incident power wave versus the system reflected power waves at the fundamental and harmonic frequencies.

This formalism makes it possible to reproduce the characteristics of the DUT subjected to the stimuli used during the extraction.

It is, therefore, tempting to use this model to predict figures of merit (FOM) associated with modulated signals such as BER or ACPR.

In practice, the evaluation of these FOMs is carried out through the time domain of the modulated signal envelope, using an adequate sampling rate, which allows the accurate description of the amplitude variations. The data-flow simulator manages the signal's time sampling.

The PHD model processes each sample under the quasi-static approximation, this means that the output signal envelope of the model at a specific time "t" is calculated from the input signal envelope at the same time.

The 2-tone data-flow simulation of a PHD model confirms that the model always predicts the same response independently from the modulation speed of the signal envelope, or in other words, the spacing between the two tones. (Fig. 4)

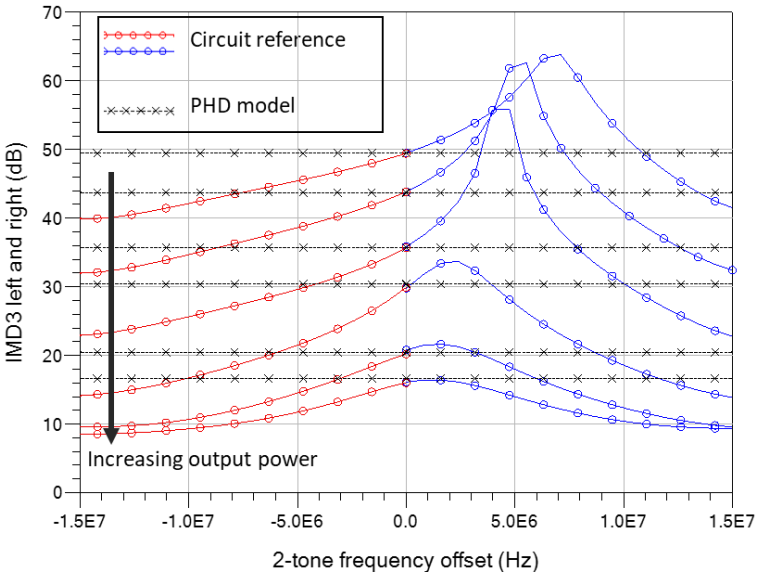

Figure 4- 2-tone simulation of a memoryless model (black)

In this case, a more advanced model is necessary to reproduce the response of a circuit presenting memory effects in a data-flow simulation environment.

An improvement of the static PHD model has been proposed [3] to better catch the memory effects, using multi-tones signals. Still, this methodology does not solve all the challenges that must be managed by system designers. Indeed, the complexity of the measurement setup prevents a broad adoption of this model in our industry. Also, the model coefficients of this multi-tones PHD model are highly correlated to the statistic of the modulated signal used for the extraction. As a result, the lack of generality prevents the model from being used with different kinds of waveforms. Finally, this model has been designed to be used only with an HB simulator, which is not optimal for an accurate bottom-up system design flow.

Limitation of PA behavioral model from data-flow simulator

Non-linear models such as the hyperbolic tangent function or the Saleh model are proposed by default in simulators to represent the behavior of the PA. These models are limited by the static system assumption

and ignore any frequency dispersion and are therefore only suitable for applications with narrowband signals.

The gain variation in the operating band of an amplifier is referred to here as HF memory effects. They are highlighted by the variation of the AM-AM and AM-PM characteristics as a function of the frequency. The system time constants for this type of memory are relatively short, similar to the carrier period.

To account for the frequency dependence, some models propose to associate static nonlinearities (Saleh, tanh, etc.) with digital filters (FIR, IIR). The association of these elementary structures forms different topologies of the HF memory model, the simplest of which are the so-called Wiener and Hammerstein models. However, using these structures is not easy, especially when it comes to identifying the filters to apply.

Beyond the effects of RF frequency dispersion or HF memory effects, power amplifiers exhibit more complex behaviors in the non-linear regime. Referred to as low frequency (LF) memory effects, these behaviors are attributed to phenomena with long time constants such as self-heating or interactions from biasing circuits. The global representation of these complex phenomena requires the use of more general mathematical formulations like the Volterra series. In practice, the Volterra series quickly become difficult to identify because of the number of coefficients. The application of this formalism is restricted to slightly non-linear systems. Nevertheless, hypotheses on the kernels of the series can be considered to reduce the complexity of the model. These formulations are known as the Generalized Memory Polynomial (GMP).

$$\begin{aligned}\tilde{y}(k) = &\sum_{p=0}^{P}\sum_{m=0}^{M}\tilde{a}_{pm}|\tilde{x}(k-m)|^{2p}\tilde{x}(k-m)\\ &+\sum_{p=1}^{P_b}\sum_{m=0}^{M_b}\sum_{v=1}^{V_b}\tilde{b}_{pmv}|\tilde{x}(k-m)|^{2p}\tilde{x}(k-m-v)\\ &+\sum_{p=1}^{P_c}\sum_{m=0}^{M_c}\sum_{v=1}^{V_c}\tilde{c}_{pmv}|\tilde{x}(k-m)|^{2p}\tilde{x}(k-m+v)\end{aligned}$$

Figure 5 – Generalized memory Polynomial

The MP and GMP models are the two most common models and exhibit excellent performances in reproducing non-linear and memory effects when the excitation signals belong to the same class of signals used for identification. In other words, the scope of this category of models is limited to the dynamics of the identification signal. It will, therefore, be necessary to extract as many models as application signals are covering the DPD algorithm tests. Also, these models offer a formalism where nonlinearity and memory effects are intimately linked in the series terms. The main difficulty lies in the large number of parameters to be estimated for the modeling of a highly non-linear device and the optimal estimation of the order of memory and nonlinearity.

The extraction of the MP and GMP models is based on the waveforms of the PA input and output signals. For wideband applications, it may be difficult or even impossible to obtain this data from either circuit simulation or measurements. Indeed, on the one hand, circuit simulation can be prohibitive in simulation time or convergence issues caused by the complexity of the circuit. On the other hand, the use of measurement data implies access over the entire evaluation period of the DPD algorithm to a dedicated measurement bench with an engineer trained in the use of high-end vector signal generators and

analyzers (VSG-VSA). The VSG must be able to provide the IQ frames of the latest standards. At the same time, the VSA must allow the analysis of the PA output signal with sufficient dynamic range and a capacity to sample at least 5 times greater than the input signal to evaluate the adequate bandwidth. These capabilities are not always available, and the required time for all the measurements is not always possible, given the time to market restrictions.

Solution

In this context, our modeling tool (VISION) [1] offers a practical solution for extracting, simulating, and exporting behavioral models to system simulators.

VISION offers different types of models, with different levels of complexity. These models take into account, among other phenomena, high frequency and/or low-frequency memory effects, thermal effects, and mismatch. Rather than extracting a model that would systematically take into account all the effects, Vision offers an interface that allows users to choose the simplest and yet most accurate model, depending on the observed phenomena and the need to take them into account or not. The aim is to optimize the complexity versus simplicity of each model and yet obtain reliable and efficient system simulation.

In the following case, we use a unilateral, high frequency, and low frequency (U-HFLF) model based on Two Path Memory (TPM) topology [4]. This model is independent of the load impedance, which is set to 50 Ohms.

The extraction of this model can be carried out from HB simulations of the circuit design.

Alternatively, VISION can control test benches composed of standard instruments, commonly used in RF laboratories, to generate necessary measurement data to extract the behavioral model of the circuit under test.

Extraction templates are provided to obtain the necessary data used by the “Device Modeler” extraction tool in VISION. These templates include all required settings and sweeps needed to stimulate the circuit design. First, a CW signal is swept in power and frequency to obtain a network of AM to AM and AM to PM curves. Second, a specific complex signal composed of 3 tones with a specific set of amplitudes, phases, and spacing is used to probe the memory of the circuit. The simulation results are then exported

in the form of 2 text files representing respectively the characteristics of the high-frequency (HF) memory response (short term memory) and the low-frequency (LF) memory response (long term memory).

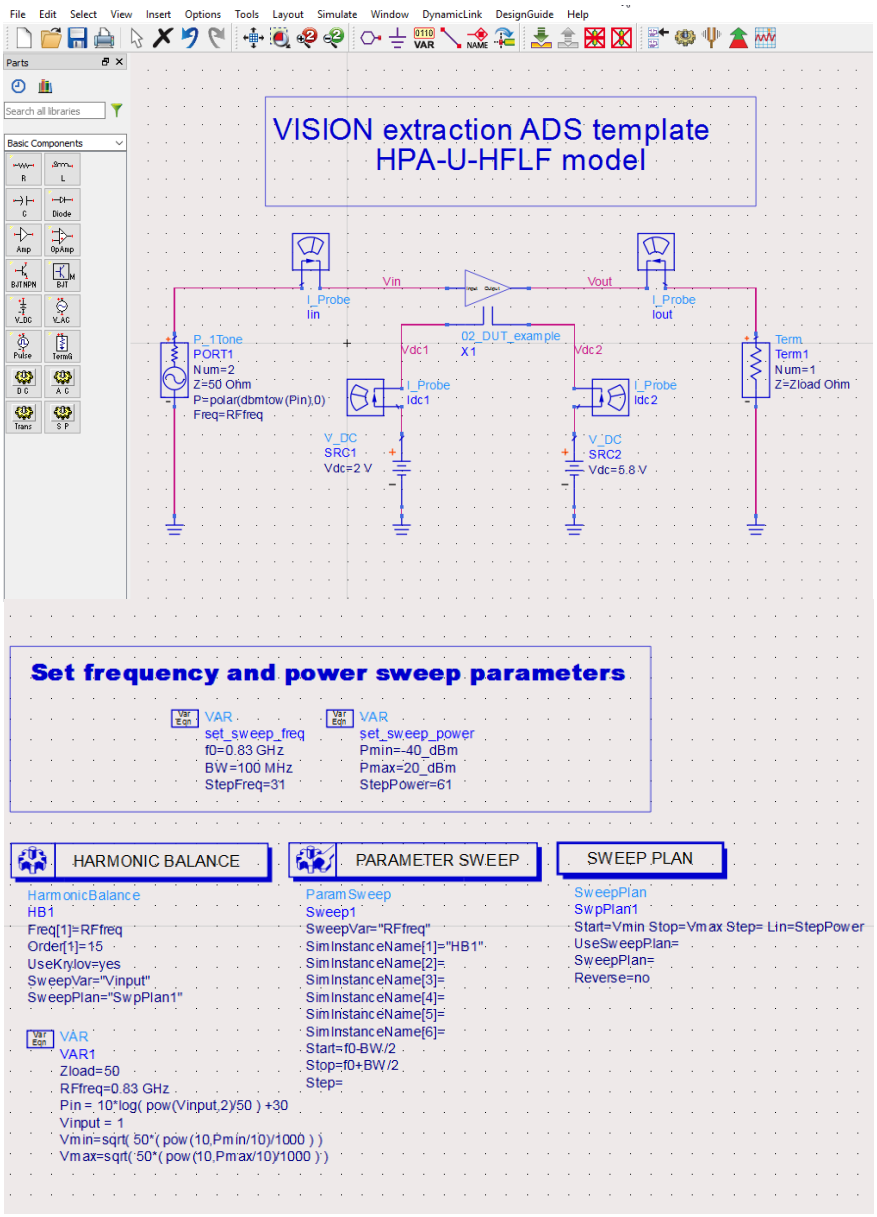

Figure 6- Extraction template using a circuit simulator (Circuit design and simulation settings)

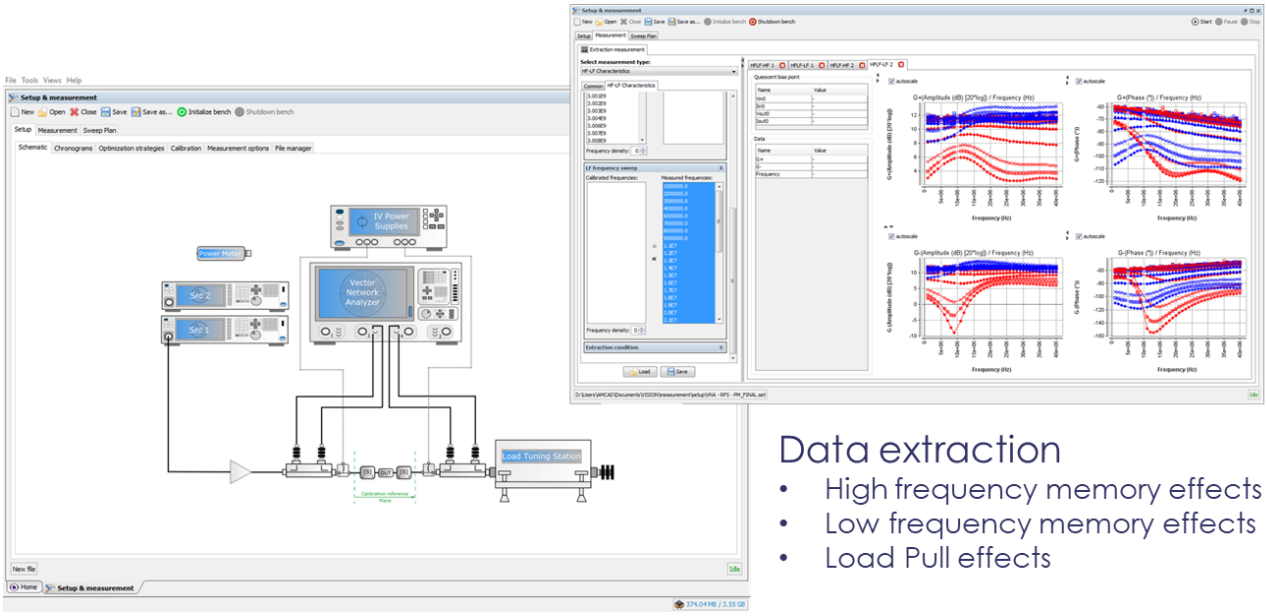

Figure 7- Bench control User Interface for behavioral model extraction

VISION model extraction

VISION "Device Modeler" uses data files obtained from simulations or measurements. It also displays a set of parameters to be adjusted to perform the extraction. The accuracy of the model can be monitored directly in the graphical tool. As such, it allows you to adjust the model extraction parameters and better fit the model simulation results with the data, if necessary (Fig. 8)

Through these steps, the circuit modeling process allows a more in-depth understanding of the circuit behavior and the impact of the memory effects on the output signal distortion.

The extracted behavioral model is automatically listed in the VISION "Device Modeler" library and made available in the VISION "System modeler" data-flow simulation environment.

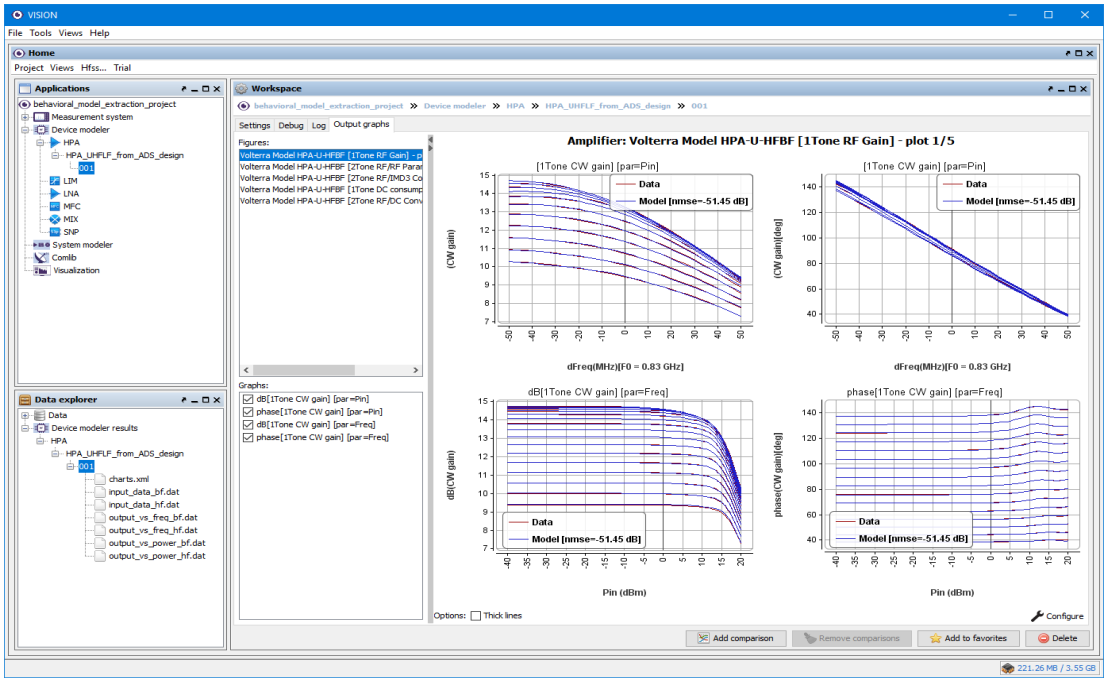

Figure 8- VISION Device Modeler tool

Simulation Results

The simulation environment of the "System Modeler" enables the possibility to test the model in time-domain and study its prediction capabilities under modulated signals stimulus. A 2-tone signal is used to simulate the model in time-domain in VISION, and results are compared with those obtained using an HB simulation of the circuit design and the data-flow simulation of a PHD model of the same circuit.

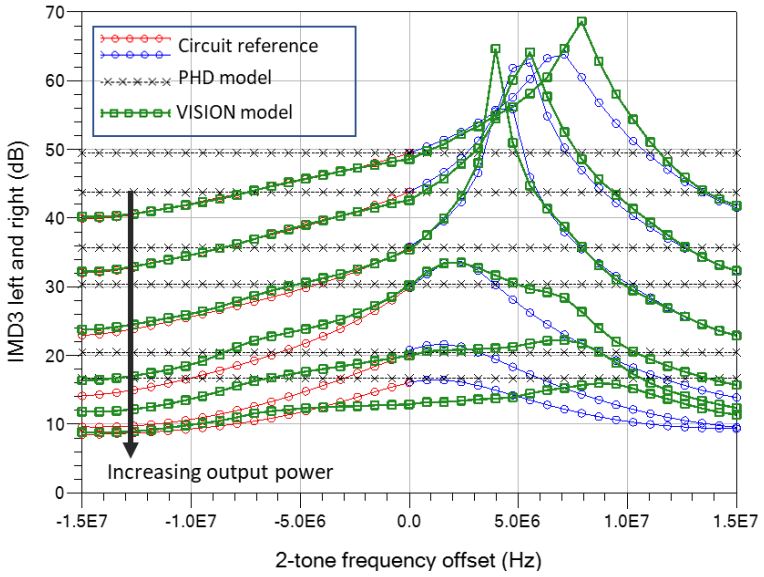

Figure 9- 2-tone simulation of the VISION HPA-UHFLF model (Bold dashed lines) versus reference simulation (Continuous line)

We observe a good match between the simulation results of the extracted behavioral model in VISION and the HB simulations, used as a reference. Also, we notice that the prediction quality of the VISION

model is better than the static PHD model proposed in the previous section. VISION model predicts the resonance due to the memory effects present in the studied power amplifier accurately.

Export feature to other system simulators

The challenge of system simulators is to address the increasingly complex systems and a large variety of analyses.

System simulators allow designers to explore several architectures and evaluate different algorithms to obtain desired performances and possibly determine, as early as possible, the compromises to be made in their design process. For that, these tools represent the design in the shape of interconnected block diagrams leading to fast simulation times. They also offer an extensive library of predefined blocks, among them, signal processing (DSP) and RF applications ones.

In the particular case of blocks representing RF circuits (PA, mixer, filter, ...), these latter are composed of ideal models, fed by system-level specifications or circuit-level figure-of-merits. A co-simulation, comprising the circuit design netlist is necessary to estimate the real effects of the blocks' imperfections on the system performances. However, complex modulated signals related to the system's final application require high sampling rates to be correctly represented during the simulation. The combination of these signals with the co-simulation mode leads to very long simulation times and makes the verification process complicated, if not impossible. In such a case, the use of behavioral modeling is essential.

System designers may also be dealing with a situation where they must integrate several circuit models, designed by different groups. Without complete compatibility between different simulation tools or their data formats, the verification process becomes tedious. This problem is a significant source of frustration in the evaluation of next-generation telecommunications system architectures.

VISION modeling tool proposes an adequate solution to this issue. It allows the export of the circuit behavioral model to heterogeneous system simulators. This option unifies the modeling methods of circuit designers and ensures the interoperability of the circuit behavioral model with most of the commercially available system simulators. Vision also offers its own schematic edition tool to evaluate system performance through data-flow simulations.

To illustrate the affirmations above, we used the PA reference circuit design, used in the sections above, comprising a transistor model with its input and output matching networks as well as the bias circuitry. The simulation is done in Harmonic Balance mode using a commercially available circuit simulator (ADS, Keysight Technologies) to predict the performances of the PA under a 64-QAM modulation signal with 14 dBm input power and a PAPR of 6 dB. This simulation allowed the excitation of the resonance observed at 5MHz in Fig. 7 due to memory effects. The total simulation time was 30 minutes.

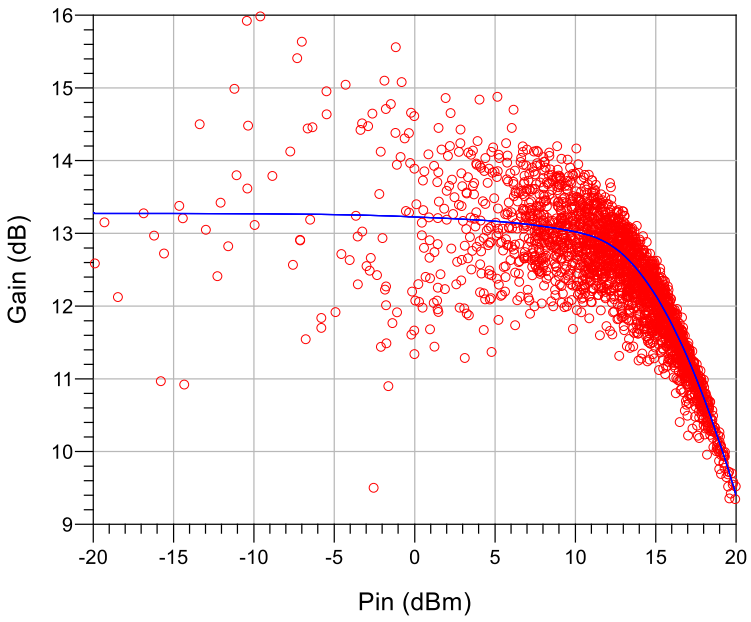

Figure 10- Dynamic AM-AM of Modulated signal (Red) and Static AM-AM for CW signal (Blue)

A memoryless PHD and a VISION U-HFLF model of the reference PA circuit are extracted and exported to a data-flow type system simulator (such as Pathwave SystemVue from Keysight Technologies) to compute the same figure of merits obtained in the simulation described in the previous paragraph.

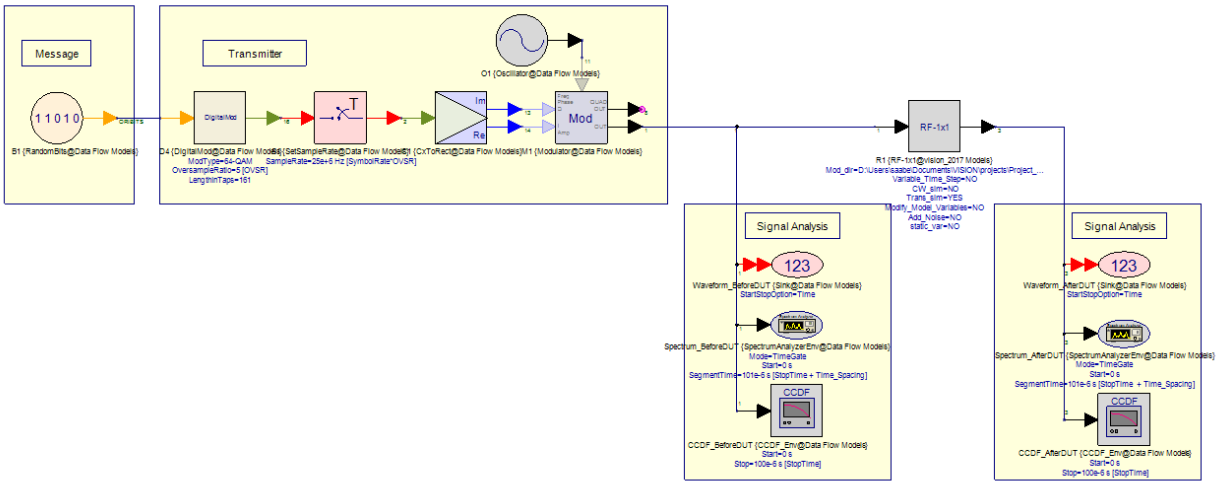

Figure 11 - Block diagram in system simulator

In this case, the simulation times for the PHD model and the VISION U-HFLF model were 5 and 30 seconds, respectively.

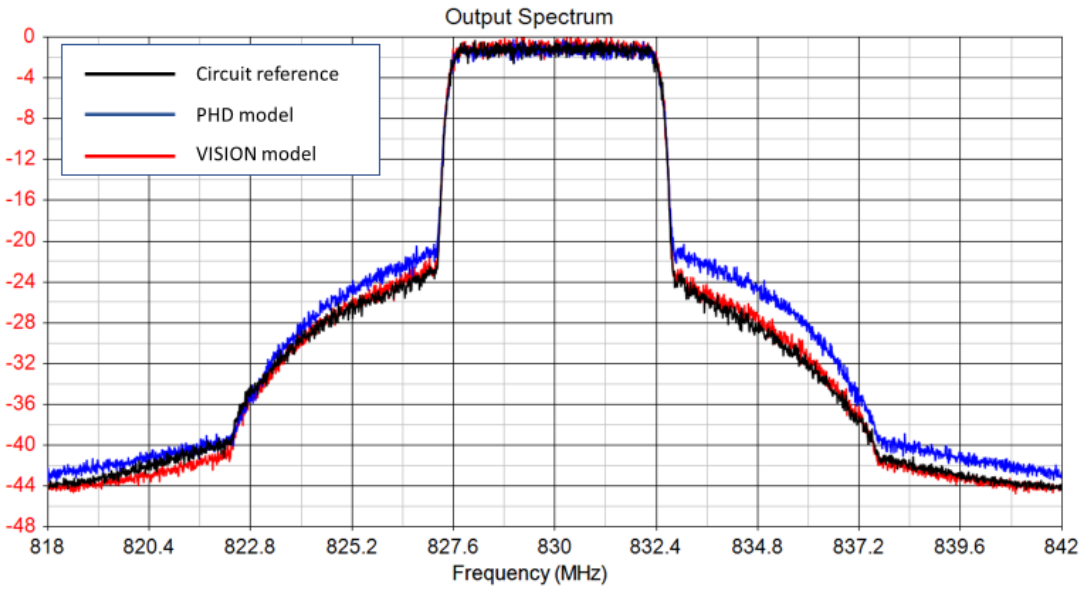

Figure 12 – Output Spectrum of the reference circuit (black), Vision Model (red) and PHD model (blue)

On top of the fast simulation time, we can observe that the static PHD model predicts a perfect symmetry between the left and right ACPR, which is not compatible with low-frequency memory effects. (Fig. 12). Also, we note that the simulated spectral regrowth on the right side is overestimated by around 5dBc compared to the circuit simulation carried out using the transistor model and matching circuits used as a reference here.

Finally, we can see that the simulation performed using the VISION model predicts the asymmetry between ACPR right, and ACPR left as expected. It shows a clear added value over the static PHD model, which does not exhibit this critical characteristic that is needed to be taken into account if the amplifier was to be linearized.

VISION U-HFLF model is not only accurate for basic stimulus like 2-Tone signals, but it is also well suited for wideband modulated signals. On the contrary, PHD models show clear limitations when used for other than CW input signals.

DPD application example

In this section, we present an example of DPD algorithm evaluation in the Simulink simulation tool (Mathworks) using the VISION model of the Power Amplifier seen previously in this paper.

In a standard design flow, the amplifier linearization problem can be addressed, either while the amplifier is being designed, or on an available on-the-shelf circuit.

For the designed circuit, the objective is to anticipate the true amplifier performances once linearized. The circuit designer can refine the architecture in a circuit simulator and applies a pre-distortion algorithm using a circuit envelope simulation on the circuit design that goes down at transistor level. The

analysis highlights figure-of-merits such as ACPR, BER, and EVM. Design adjustments can still be made, such as adjusting the video bandwidth by optimizing the bias circuits of the transistor. Although this methodology has the advantage of predicting the real linearity performance of the amplifier once it is linearized, the simulation time is extremely long (potentially up of to several hours depending on the signal bandwith).

Also, it does not allow designers to have an efficient design and optimization process. In this case, the circuit-level behavioral model extraction and export to a data-flow type system simulator makes it possible to significantly shorten the simulation time, and observe the performances of the linearized amplifier, without losing the precision required on the estimation of circuit performance.

The other application case is when the designer has the finalized amplifier and wishes to optimize its linearity using digital pre-distortion of the baseband signal. It is, therefore, necessary to develop and optimize the DPD algorithms to obtain the best linearity performance. Power amplifier vendors have to show how their circuits perform once linearized to differentiate themselves from competitors. Therefore, this point becomes critical, especially when wideband signals are used.

In practice, these algorithms are developed on a test bench, where it is necessary to control the test bench using analog and digital signals. Turnkey test instruments facilitate this characterization process, like the Vector Signal Transceiver (VST), using an observation path and an on-board FPGA, can optimize the coefficients of the live linearizer model to optimize DUT performances. Thanks to turnkey measurement software solutions, such as IQSTAR, a software solution developed by AMCAD for Power Amplifier Characterization [8], the user can, therefore, adjust the memory depth of the pre-distortion model, its non-linear description order, and observe the linearity performance of the amplifier in real-time.

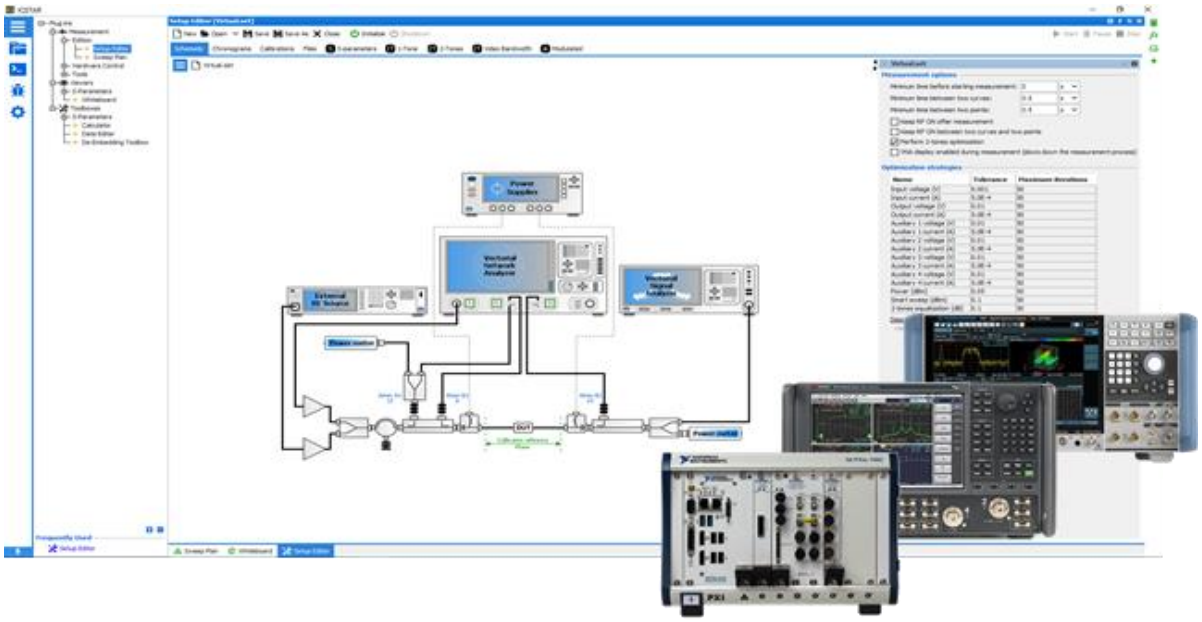

Figure 13 :IQSTAR allows simple control of complex characterization bench architectures with different hardwares

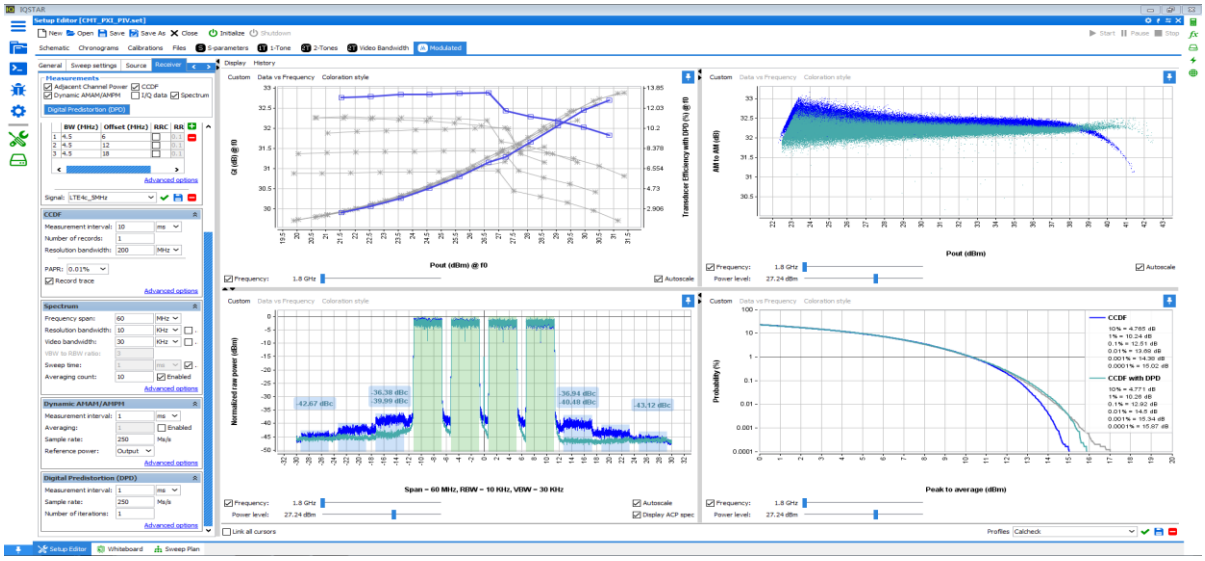

Figure 14 : IQSTAR optimizes the generalized memory polynomial model parameters for Digital Pre-Distortion

This solution allows the designer to easily perform pre-distortion tests on an amplifier, without requiring any special skills in programming on-board electronics. Although useful to predict the power performances of the linearized amplifier (AM-AM and AM-PM), these tests cannot forecast the overall consumption. Indeed, the digital circuit, which is implemented alongside the amplifier, consumes energy as well. This consumption is increasing with the bandwidth of the pre-distorted signals. It is, therefore, important that the chosen linearization algorithm is also compatible with the implementation of power efficient on-board electronic circuits.

Suppliers of System on Chip (SoC) offer nowadays agile and integrated RF transceivers solutions dedicated to communication signals [9] [10]. The implementation of such solutions requires specific skills to program the on-board electronics and be able to develop and evaluate different linearization algorithms.

Indeed, the implementation of DPD algorithms in SoC for RF system requires a pool of expertises :

Proficiency within the field of signal processing, telecommunication systems and radio technology

Systemization knowledge of combined hardware, firmware, middleware and software domains

Radio systemization experience in requirement setting for GSM, WCDMA, LTE and NR

Experiences on systemization of radio DPD (Digital Pre-Distortion), PIMC (Passive Inter-Modulation Cancellation), DAC/ADC (Digital-Analog Converter/Analog-Digital Converter)

Knowledge in embedded systems, system-on-chip, ASIC, FPGA

The required skills and the technical means necessary for the implementation of this process may call for significant resources for the development. This different skills are required by companies which are developing telecommunication systems. But, for the PA vendor, having all these skills can be questionable. As a matter of fact, the power amplifier vendor can be led to communicate on the performances of his linearized system, relying only on standard techniques and models, without being able to demonstrate the true potential of his system under optimal linearization techniques.

The aim of behavioral modeling solutions is to propose a solution that can reveal the true Power Amplifier performances during the simulation process when optimized with state of the art DPD algorithms.

The application proposed below offers circuit designers a new methodology in their design flow. It helps optimize their linearization algorithms, without being limited by the technical implementation, and yet anticipate the optimal performance of their circuit realistically once linearized.

The concept is to extract a behavioral model of an amplifier, using data from measurements or circuit simulation, and to apply different linearization algorithms to optimize the baseband and RF performances of the circuit in a system simulation tool.

Our goal is to illustrate the importance of using a reliable behavioral model, taking into account all memory effects, during this design phase using EDA tools.

First, we compare a U-HFLF model extracted using the VISION modeling platform with a memoryless model. These two models are simulated in Mathworks Simulink using two signals with 5 MHz and 20 MHz bandwidth, respectively.

Note that these bandwidths are not representative of 5G-NR ultra-wideband signals, due to the limitation of the video band of the reference amplifier chosen in this example. However, this same concept would be applicable with wider band amplifiers, for which the linearization would become a real challenge.

The signal contains 50,000-time samples and is based on a 64QAM modulation. We observe that the asymmetry between the left and right spectral lifts becomes more pronounced in the case of the VISION U-HFLF model when the signal bandwidth is increasing, which is a characteristic of the LF memory present in the circuit (Fig. 2). On the other hand, the spectrum of the simplified memoryless model offers symmetrical performances (Fig. 16).

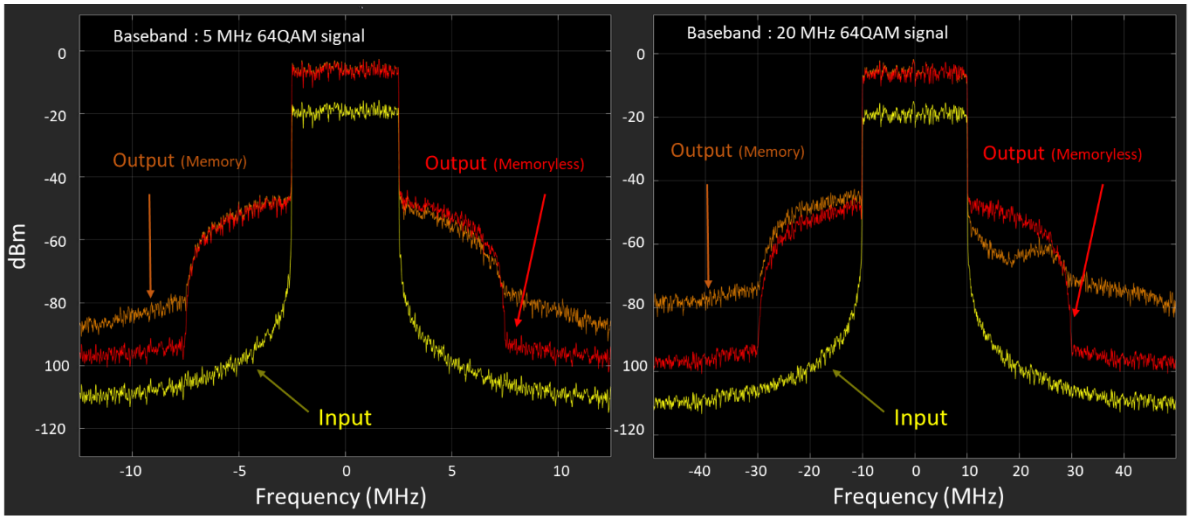

Figure 16 – Input &output spectrum using the VISION model (orange) and memoryless model (red)

Concerning the DPD assessment, the diagram, presented in Figure 16, was carried out with the following elements:

- The VISION U-HFLF model and a memoryless model of the PA;

- DPD represented by the GMP behavioral model;

- The DPD coefficients estimation algorithm using the "Recursive Least Squares" (RLS) method.

It should be noted that the algorithm used is only for illustration and does not guarantee the best linearity performances, but it does illustrate the proposed benefits.

Research on DPD algorithms is a research subject in its own right, which today mobilizes research teams specialized in this field [11-12]

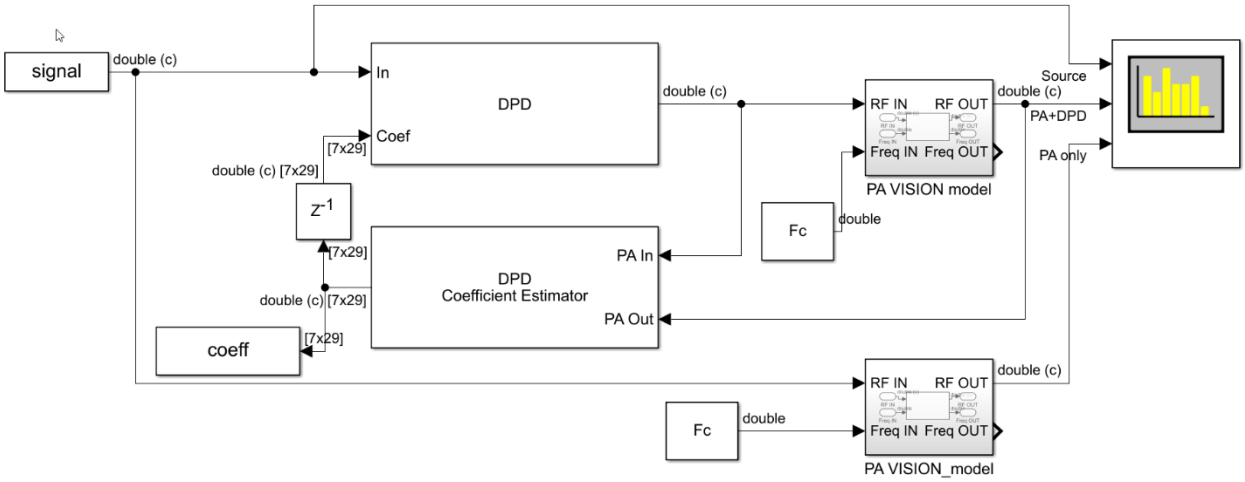

Figure 17 - Simulink schematic used to simulate the DPD

At the end of the simulation, we can compare the PA input and output signal spectrums with and without DPD. The GMP model orders used in the DPD is 5 for nonlinearity and 7 for the memory depth for the two cases, leading to 145 coefficients calculation.

We observe that for the signal with 5 MHz of bandwidth, the DPD reduces the spectral distortion of the signal, for both amplifier models (Figures 18).

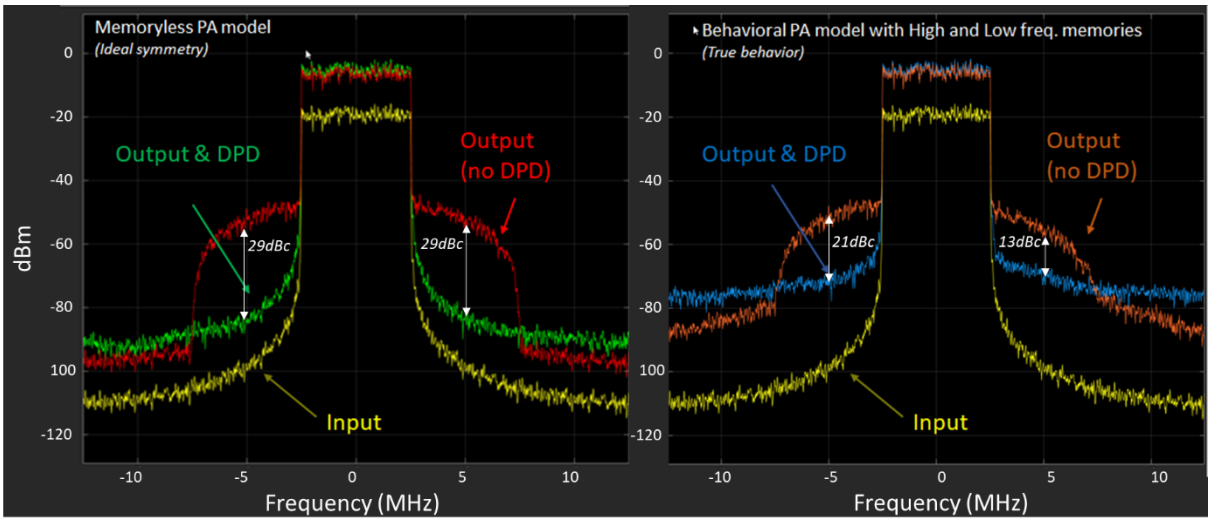

Figure 15 - Input and output spectrum for 5 MHz 64QAM signal

In this first case, we can already observe that the DPD algorithm applied to a simplified model would overestimate the performance of the result obtained in terms of linearity, and would not allow us to observe the asymmetry in adjacent channels.

The DPD algorithm used in this case would not deliver the performances expected on the linearization of the amplifier when using a simplified model.

When the signal bandwidth is increased to 20MHz, on the left handside, the DPD manages to reduce the distortion of the memoryless-based amplifier model (Fig. 19). However, on the right handside, under the same conditions, the algorithm fails to linearize the VISION TPM-based amplifier model and, on the contrary, tends to worsen it.

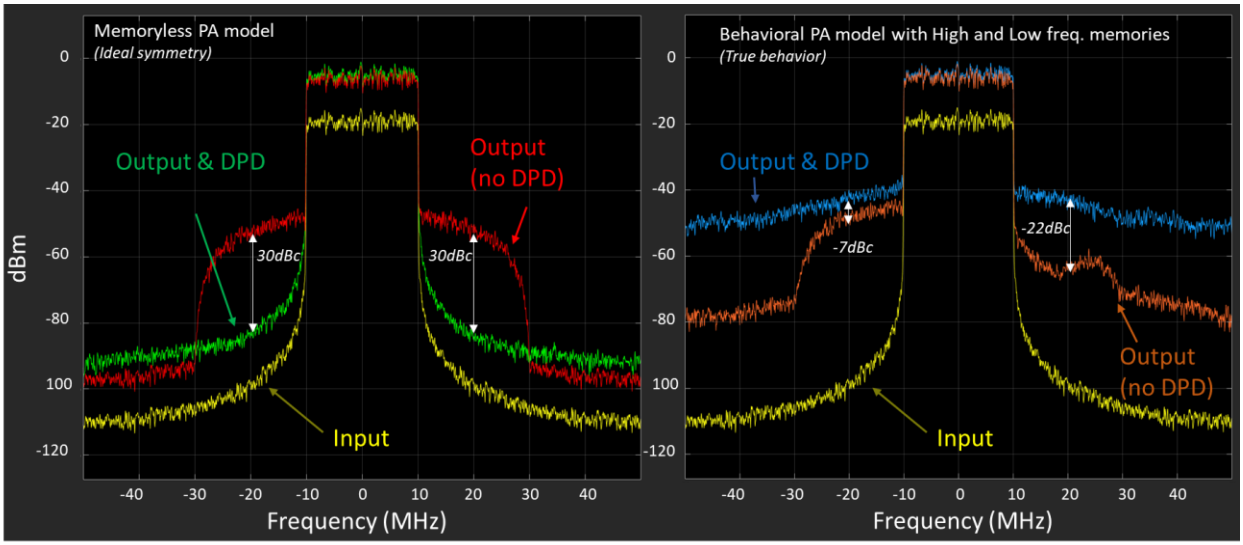

Figure 16 - Input & output spectrum for 20 MHz 64QAM signal

Conclusion

In this paper, we intended to explain the strengths and weaknesses of memoryless behavioral models, such as PHD models. We also presented a better fitting solution to system designers and in-line with their design needs.

Indeed, during a top-down type design phase, the system specifications must be broken down into circuit-level ones. For that, the PHD model comes handy to evaluate such specifications as it is possible to simulate the non-linear response of the circuit using a CW signal. The basic figures-of-merits for RF designer (power, gain, NF, …) can be predicted with basic behavioral models for each circuit comprised in the system architecture.

On the other hand, when the advanced validation of the system under modulated signals is required, and when the simulation results must represent, in a reliable way, the performances of the overall system, including the baseband, then taking into account the memory effects and its behavior becomes a “Must-to-have.” The possibility to predict the memory effects of a circuit allows the evaluation and simulation of correction techniques using digital baseband signal processing.

We saw in this example that the behavioral model extracted using the VISION tool is a unique solution that provides high confidence in the obtained results and allows a better assessment of the system performance.

The VISION U-HFLF model provides valuable information required by engineers to design complex RF system architectures, such as linearized amplifiers or active antennas, for which the baseband signal digital processing contributes significantly to the system performance.

To describe the memory effects and correctly evaluate the performance of DPD systems in simulation, it is therefore mandatory to use amplifiers' behavioral models, which take into account low and high-frequency memory effects. Indeed, the use of a simplified model would not make it straightforward to linearize and would lead to an implementation of inefficient algorithms.

Besides, unlike the commonly used amplifier behavioral models, the VISION platform makes it possible to provide precise and valid models, whatever the statistics of the modulation used in baseband, and whatever the compression level of the amplifier. There is no need to re-extract the coefficients from the model when the back-off conditions or the bandwidth are changed.

By providing robust and reliable models and allowing the implementation of fast system simulation, AMCAD VISION behavioral modeling solution for data-flow system simulation offers tools that open new perspectives to improve the linearity performance of communication systems, allowing our partners to enhance the value proposition of their power amplifier circuits.

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